Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3357	(trench or recess or hole or opening or aperture) and ((optical or optically) with isolation)	US-PGPUB; USPAT	OR	ON	2005/03/16 10:51
L2	2150	(trench or recess or hole or opening or aperture) and ((optical or optically) near5 isolation)	US-PGPUB; USPAT	OR	ON	2005/03/16 10:43
L3	41	(trench or recess or hole or opening or aperture) and (((optical or optically) near5 isolation) same (polysilicon or titanium or aluminum or tungsten))	US-PGPUB; USPAT	OR	ON	2005/03/16 10:46
L4	41	3 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 10:52
L6	19	(trench or recess or hole or opening or aperture) and (((optical or optically) near5 isolating) same (polysilicon or titanium or aluminum or tungsten))	US-PGPUB; USPAT	OR	ON	2005/03/16 10:46
L7	18	6 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 11:11
L8	17	7 not 3	US-PGPUB; USPAT	OR	ON	2005/03/16 10:46
L10	437	(trench) and ((optical or optically) with isolation)	US-PGPUB; USPAT	OR	ON	2005/03/16 11:11
L11	421	10 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 10:52
L12	48	(trench) and ((optical or optically) with isolation)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/16 11:07
L13	66	(trench) and ((optical or optically) with isolating)	US-PGPUB; USPAT	OR	ON	2005/03/16 11:11
L14	58	13 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 11:11
L15	36	14 not 11	US-PGPUB; USPAT	OR	ON	2005/03/16 11:11

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	(("5,394,005") or ("5,763,315") or ("6,239,434") or ("6,303,413")).PN.	US-PGPUB; USPAT	OR	OFF	2005/03/16 14:29
L2	7970	((wafer or substrate) with (silicon adj carbide))	US-PGPUB; USPAT	OR	ON	2005/03/16 14:39
L3	105	2 and trench and (pixels or photodiodes)	US-PGPUB; USPAT	OR	ON	2005/03/16 14:30
L4	96	3 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 15:01
L5	674	((wafer or substrate) with (silicon adj carbide) with (gallium adj nitride))	US-PGPUB; USPAT	OR	ON	2005/03/16 14:40
L6	590	5 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 14:40
L7	13	6 and (trench with isolation)	US-PGPUB; USPAT	OR	ON	2005/03/16 14:59
L8	7	(optical or optically) with polysilicon with lpcvd	US-PGPUB; USPAT	OR	ON	2005/03/16 15:00
L9	812	polysilicon with lpcvd with temperature	US-PGPUB; USPAT	OR	ON	2005/03/16 15:01
L10	791	9 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2005/03/16 15:01
L12	781	10 and (deposition or depositing)	US-PGPUB; USPAT	OR	ON	2005/03/16 15:02
L13	772	12 and substrate	US-PGPUB; USPAT	OR	ON	2005/03/16 15:02
L14	159	13 and (trench with polysilicon)	US-PGPUB; USPAT	OR	ON	2005/03/16 15:02

DOCUMENT-IDENTIFIER: US 20020153529 A1

TITLE: LED array with **optical isolation** structure and method of manufacturing the same

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

A Light Emitting Diode array (LED) with an **optical isolation** structure and a method of manufacturing the same. The LED array with an **optical isolation** structure includes a substrate, a plurality of LED units and a plurality of trenches. The plural LED units and trenches are disposed on the surface of the substrate. Each trench is disposed between every two LED units and deposited with at least one reflective metal layer. The substrate of the LED array with an **optical isolation** structure is formed of a low-energy-gap semiconductor material, while the LED units are formed by another kind of semiconductor material whose energy gap is higher than the substrate. The light emitted from each LED unit is reflected by the plural trenches deposited with at least one reflective metal layer, and absorbed by the substrate with low-energy gap.

Title - TTL (1):

LED array with **optical isolation** structure and method of manufacturing the same

Summary of Invention Paragraph - BSTX (3):

[0002] The present invention relates to an LED array for the LED display or the LED printer and the method of fabrication the same. Especially, the present invention is about an LED array with an **optical isolation** structure and a method fabricating thereof with a reduced cost.

Summary of Invention Paragraph - BSTX (10):

[0008] Therefore, one object of the present invention is to provide a LED array chip with an **optical isolation** structure, which prevents the light emitted from each LED pixel from transmitting into the areas of neighboring LEDs and increases the image resolution thereof.

Summary of Invention Paragraph - BSTX (11):

[0009] Further, another object of the present invention is to provide a method of fabricating a LED array with an **optical isolation** structure. The LED array is constructed by forming a plurality of LED units on the same substrate

with a semiconductor process. The complicated packaging process is simplified and therefore, the cost of LED array manufacturing process is reduced.

Summary of Invention Paragraph - BSTX (12):

[0010] According to the present invention, the LED array with an **optical isolation** structure includes a substrate, a plurality of LED units and a plurality of trenches. The substrate is made of a semiconductor material with low energy gap. The plural LED units are formed on the substrate, and each LED unit having a PN junction layer made of a semiconductor material whose energy gap is higher than the substrate. The plural trenches are formed on the substrate. Each trench is disposed between every two adjacent LED units, and the depth of each trench is larger than the that of the LED junction. A first insulation layer is deposited on the entire surface of the substrate, including the surface of each LED unit and each trench. A first reflective metal layer is deposited on the surface inside each trench, and overlaid on the first insulation layer formed inside each trench. A second insulation layer is deposited on the surface of the first reflective metal layer formed inside each trench, and is used to refill each trench and planarize the entire surface of the substrate. A passivation layer is formed on the entire surface of the substrate. A plurality of contact windows are formed on the surface of the plural LED units. Each contact window is etched through the passivation layer and the first insulation layer deposited on each LED unit, and is used to expose part of the PN junction layer of each LED unit for electrical connectivity. A plurality of metal bonding pads are formed on the substrate, and connected to the surface of the PN junction layer inside the plural contact windows. And, a backside metal layer is formed on the backside of the substrate for one of the external electrical conduction.

Brief Description of Drawings Paragraph - DRTX (5):

[0017] FIG. 4 is a cross-sectional view illustrating a 2.times.N LED array of the preferred embodiment possesses the advantage of **optical isolation** according to the present invention;

Detail Description Paragraph - DETX (3):

[0021] Therefore, the present invention is to provide a LED array with an **optical isolation** structure that avoids the cross-talk phenomenon in the traditional LED array by utilizing the trench technology in semiconductor process. Now, the LED array according to the preferred embodiment of the present invention and the method of fabricating the same will be described below.

Detail Description Paragraph - DETX (9):

[0027] Then, the process of constructing an **optical isolation** structure in a 2.times.N LED array or a N.times.N LED array according to the present embodiment is described below.

Detail Description Paragraph - DETX (14):

[0032] According to descriptions mentioned above, the first insulation layer 204, the first reflective metal layer 205 and the second insulation layer 206 are constructed in the plural net-like the trenches 203 disposed between the plural LED units and thus constitute an **optical isolation** structure on the substrate 201. The depth of the **optical isolation** structure, in which a first reflective metal layer 206 is provided, is larger than the depth of the PN junction layer 202 of the plural LED units. Consequently, when the light emitting from each LED unit transfers toward the transverse directions of the unit, namely T-rays, the light transmits through the first insulation layer 204 next to the emitting LED unit, and irradiates on the first reflective layer 205 next to the insulation layer 204. Then, the light is reflected by the first reflective metal layer 205, and returns back into the area of the original emitting LED unit. Further, the substrate of the LED array of the present embodiment is made of the material whose energy gap is lower than the material of the PN junction layer of the plural LED units, i.e. the substrate is made of GaAs, and the PN junction layer is made of AlGaAs. Therefore, when the light emitting from each LED unit and transfers downwardly, namely B-rays, is absorbed by the substrate 201 whose low energy gap. Thus, the cross-talk phenomenon in the traditional LED arrays is avoided by the **optical isolation** structure of the LED array of the present invention successfully.

Claims Text - CLTX (2):

1. A light emitting diode array with an **optical isolation** structure, comprising: a substrate made of a semiconductor material; a plurality of light emitting diode units formed on said substrate, therein, each light emitting diode unit having a PN junction layer made of a semiconductor material whose energy gap is higher than said substrate; a plurality of trenches formed on said substrate, each trench is located between every two adjacent said light emitting diode units and used to isolate said adjacent plural light emitting diode units, therein, the depth of said trenches is larger than the depth of said light emitting diode units; a first insulation layer formed on said substrate, said first insulation layer is formed on the surface of said plural light emitting diode units and on the surfaces inside said plural trenches; a first reflective metal layer formed on said substrate, said first reflective metal layer is formed on the surface inside said plural trenches and overlaid on the first insulation layer formed inside said plural trenches a second

DOCUMENT-IDENTIFIER: US 20040089914 A1

TITLE: Isolation techniques for reducing dark current in CMOS image sensors

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (6):

[0004] In a CMOS image sensor, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge from the floating diffusion node. Photo charge may be amplified when it moves from the initial charge accumulation region to the floating diffusion node. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The photosensitive element of a CMOS image sensor pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate. A photon impinging on a particular pixel of a photosensitive device may diffuse to an adjacent pixel, resulting in detection of the photon by the wrong pixel, i.e. cross-talk. Therefore, CMOS image sensor pixels must be isolated from one another to avoid pixel cross talk. In the case of CMOS image sensors, which are intentionally fabricated to be sensitive to light, it is advantageous to provide both electrical and **optical isolation** between pixels.

DOCUMENT-IDENTIFIER: US 20030186073 A1

TITLE: Heterointegration of materials using deposition and bonding

---------- KWIC ---------

Detail Description Paragraph - DETX (22):

[0034] All of the provided examples exemplify semiconductor/semiconductor bonding. However, other materials present on the wafer surface can be present as well and included by bonding into the structure. For example, instead of bonding only to bare Si surfaces, the epitaxial wafer can be bonded to a Si wafer coated with SiO.sub.2. Using the process described, a thin GaAs/SiO.sub.2/Si structure is created, which is very useful for optical interconnects. The SiO.sub.2 layer allows for both **optical** and electronic **isolation** of the top optoelectronic layer. An example of bonding a relaxed SiGe alloy on Si to SiO.sub.2/Si is shown in FIG. 6. FIG. 6 is a cross-section transmission electron micrograph of an exemplary SiGe/SiO.sub.2/Si structure. The process used to create the material is the same as shown in FIGS. 3A-3D, except the SiGe has been bonded to a Si wafer with SiO.sub.2 on its surface.

DOCUMENT-IDENTIFIER: US 20020074556 A1

TITLE: GaN based group III-V nitride semiconductor light-emitting diode and method for fabricating the same

---------- KWIC ---------

Application Filing Date - APD (1):
20011212

Summary of Invention Paragraph - BSTX (9):
[0008] FIG. 3 shows another conventional GaN based III-V nitride semiconductor laser diode in which an n-type electrode and a p-type electrode are arranged to face opposite directions with an active layer therebetween. An n-type GaN layer 12, an n-type AlGaN/GaN layer 24, an n-type GaN layer 26, an InGaN layer 28 acting as an active layer, a p-type GaN layer 30, a p-type AlGaN/GaN layer 32, and a p-type GaN layer 36, a passivation layer 34, and a p-type electrode 38 are sequentially formed on a **silicon carbide** (SiC) **substrate** 10a (or a **gallium nitride** (GaN) **substrate**). An n-type electrode 14a is formed on the bottom of the SiC substrate 10a.

Detail Description Paragraph - DETX (99):
[0139] In particular, as shown in FIG. 44, in forming the via hole 332 in the high-resistant substrate 300, at the same time a **trench** 334 for device **isolation** can be formed in the boundary region between light-emitting devices. By doing so, a separate diamond cutting process for device **isolation** is not necessary, and the light-emitting devices can be separated by pushing the opposite side to the side where the **trench** 334 is formed. In FIG. 44, reference character A denotes a region where a light-emitting diode is formed.

US-PAT-NO: 5498566

DOCUMENT-IDENTIFIER: US 5498566 A

TITLE: Isolation region structure of semiconductor device and method for fabricating the same

---------- KWIC ---------

Abstract Text - ABTX (1):

An isolation region structure of a semiconductor device and a method for fabricating the same using both a buried oxide isolation technique and a local oxidation of silicon technique, thereby capable of having an advantage of high integrity. In the isolation region structure, narrow trenches are filled only with a **polysilicon** film whereas wide trenches are filled with a field oxide film and a **polysilicon** film so as to isolate adjacent active regions from each other. The isolation region structure includes a plurality of trenches including narrow ones and wide ones formed in the silicon substrate, a thin oxide film formed on a bottom surface and opposite side surfaces of each of the narrow trenches and opposite side surfaces of each of the wide trenches, a thick field oxide film formed on a bottom surface of each of the wide trenches, a thin nitride film formed to cover the entire surface of a portion of the thin oxide film disposed in each of the narrow trenches, opposite side surfaces of a portion of the thin oxide film disposed in each of the wide trenches and opposite edges of a portion of the thick field oxide film disposed in each of the wide **trenches, a polysilicon** film filling the narrow trenches and the wide trenches, another thick field oxide film formed over the **polysilicon** film, and a thin pad oxide film formed over the active regions.

Brief Summary Text - BSTX (40):

Therefore an object of the invention is to provide an isolation region structure of a semiconductor device and a method for fabricating the same, capable of solving the above-mentioned problems encountered in use of CVD oxide film by filling **trenches with polysilicon**.

Brief Summary Text - BSTX (42):

In accordance with another aspect, the present invention provides a method for fabricating an isolation region structure in a semiconductor device, comprising the steps of: sequentially forming a first pad oxide film and a first nitride film over a silicon substrate; patterning said first nitride film

and said first pad oxide film to expose said silicon substrate at its portion not disposed at active regions; etching said exposed portion of the silicon substrate to form a plurality of trenches including narrow ones and wide ones; forming a second pad oxide film on a bottom surface and opposite side surfaces of each of said trenches; forming a second nitride film over the entire exposed surface of the resulting structure; depositing an oxide film over said second nitride film and etching back said oxide film such that said oxide film remains to fill said narrow trenches and form spacers respectively on side walls of said wide trenches while the silicon substrate is exposed at its portions respectively disposed in the wide trenches; dipping the remaining oxide film in a HF solution to remove it; growing a first field oxide film over said exposed portions of the silicon substrate in the wide trenches by use of a primary field oxidation process; thickly forming a **polysilicon** film over the entire exposed surface of the resulting structure to fill all the **trenches with said polysilicon** film; etching the **polysilicon** film such that said **polysilicon** film remains to fill the narrow and wide trenches completely; forming a second field oxide film over the **polysilicon** film by use of a secondary field oxidation process; and removing the nitride film remaining the first pad oxide film at said active regions.

Detailed Description Text - DETX (3):

As shown in FIG. 2, the isolation region structure includes a plurality of trenches including narrow ones 51a and 51b and wide ones 51c and 51d formed in the silicon substrate 41, an oxide film 53 formed on the bottom surface and opposite side surfaces of each of the narrow trenches 51a and 51b and opposite side surfaces of each of the wide trenches 51c and 51d, and a field oxide film 59 formed on the bottom surface of each of the wide trenches 51c and 51d. The isolation region structure further includes a **polysilicon** film 61 filling the narrow trenches 51a and 51b and the wide trenches 51c and 51d, an oxide film 43 formed over active regions 49, and a thin oxide film 63 formed over the **polysilicon** film 61 to protect the **polysilicon** film 61.

Detailed Description Text - DETX (4):

In this structure, the narrow trenches 51a and 51b are filled only with the **polysilicon** film 61 whereas the wide trenches 51c and 51d are filled with the field oxide film 59 and the **polysilicon** film 61 so as to isolate adjacent active regions from each other.

Detailed Description Text - DETX (6):

As shown in FIG. 3, the isolation region structure includes a plurality of trenches including narrow ones 51a and 51b and wide ones 51c and 51d formed in the silicon substrate 41, an oxide film 53 formed on the bottom surface and

opposite side surfaces of each of the narrow trenches 51a and 51b and opposite side surfaces of each of the wide trenches 51c and 51d, and a field oxide film 59 formed on the bottom surface of each of the wide trenches 51c and 51d. The isolation region structure further includes a nitride film 55 formed to cover the entire surface of the portion of oxide film 53 disposed in each of the narrow trenches 51a and 51b, opposite side surfaces of the portion of oxide film 53 disposed in each of the wide trenches 51c and 51d and opposite edges of the portion of oxide film 59 disposed in each of the wide trenches 51c and 51d, a **polysilicon** film 61 filling the narrow trenches 51a and 51b and the wide trenches 51c and 51d, an oxide film 43 formed over active regions 49, and a field oxide film 65 formed over the **polysilicon** film 61 to protect the **polysilicon** film 61.

Detailed Description Text - DETX (19):

The nitride films 45 and 55 for the oxidation mask are dipped in a hot phosphoric acid (H.sub.3 PO.sub.4) solution of a temperature of 160.degree. C. so as to be completely removed, as shown in FIG. 4G. A **polysilicon** film 61 is then deposited over the entire exposed surface of the resulting structure by use of the **LPCVD** process at a **temperature** of 550.degree. to 650.degree. C. The polysilicon film 61 has a thickness of 5,000.degree. for filling all the trenches sufficiently and thus providing a planar surface.

Detailed Description Text - DETX (21):

As a result, the narrow trenches 51a and 51b are filled with the **polysilicon** film 61 to insulate adjacent active regions 49. On the other hand, the wide trenches 51c and 51d are filled with the field oxide film 59 formed on the bottom surfaces of trenches by use of the LOCOS process and the **polysilicon** film 61 to insulate adjacent active regions 49.

Detailed Description Text - DETX (22):

Thereafter, the surface of **polysilicon** film 61 filling the trenches is subjected to an oxidation for forming a thermal oxide film 63, as shown in FIG. 4I. As a result, the entire surface of silicon substrate 41 is covered with the oxide film. Where the surface of polysilicon film 61 is exposed, a parasitic phenomenon between an interconnection line and a gate line extending along the surface of a device finally produced occurs, thereby resulting in an increase in parasitic capacity or a formation of leakage paths. The thermal oxide film 63 on the polysilicon film 61 serves to make the polysilicon film 63 have a passivation surface for preventing an occurrence of the parasitic phenomenon.

Detailed Description Text - DETX (23):

In this embodiment, the thermal oxide film 63 having a small thickness is used as the passivation layer for the **polysilicon** film 61 filling the trenches.

Detailed Description Text - DETX (28):

Thereafter, the surface of **polysilicon** film 61 filling the trenches is subjected to a field oxidation for forming a thick field oxide film 65 capping the **polysilicon** film 61, as shown in FIG. 5I. At this time, the nitride film 55 is still left in the trenches. As a result, the oxide film 53 and the nitride film 55 serve to relieve a stress generated upon forming the thick field oxide film 65. The capping field oxide film 65 has a thickness of 500 to 3,000 .ANG..

Detailed Description Text - DETX (32):

First, the problem of crystal defect occurring at trench corners can be solved because the **polysilicon** film is deposited in the trenches at a temperature of 550.degree. to 650.degree. C. lower than that of the conventional method. In accordance with the conventional method, crystal defect occur at lower corners of trenches because the CVD oxide film fills the trenches at a high temperature of 750.degree. to 800.degree. C.

Detailed Description Text - DETX (33):

Second, a problem of a stress generated at a heat cycle process step following the formation of isolation regions can be solved because the trenches are filled with the **polysilicon** film exhibiting the same thermal expansion coefficient as the silicon substrate. In accordance with the conventional method using the CVD oxide film exhibiting the thermal expansion coefficient different from the polysilicon film, a stress is generated at the heat cycle process step, thereby occurring crystal defect.

Claims Text - CLTX (11):

forming a **polysilicon** film to fill the narrow and wide trenches;

Claims Text - CLTX (34):

(k) forming a **polysilicon** film to thereby fill the narrow and wide trenches;

US-PAT-NO: 6547146

DOCUMENT-IDENTIFIER: US 6547146 B1

TITLE: Method, system and apparatus for processing barcode data

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Detailed Description Text - DETX (18):

A transparent window 57 can be fitted over the open end 60 to enclose the compartment 62. A **photoemitter** 56, such as a commercially-available IR light emitting diode (LED), and a photodetector 58, such as a commercially-available phototransistor, are disposed at one end of the enclosed elongated compartment 62 so that their **photosensitive** surfaces generally face the open end 60.

Detailed Description Text - DETX (24):

FIG. 3 illustrates an embodiment of the present invention where the **photosensitive** surfaces 71, 72 of the **photoemitter** 56 and photodetector 58 are not aligned with the optical axes of the illuminator and imaging lenses 52, 54. In an alternative embodiment, the axis of the **photoemitter** 56 can be aligned with the optical axis of the illuminator lens 52, while the **photosensitive** area of the photodetector 58 can be aligned so that it is substantially normal to the optical axis of the imaging lens 54.